REMARKS

Double Patenting Rejection

Claims 1-30 were rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-37 of U.S. Patent No. 6469932. Applicant respectfully traverses this rejection.

In rejecting claims 1-30 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-37 of the '932 Patent, the Examiner stated that "[a]lthough the conflicting claims are not identical, they are not patentably distinct from each other. For example, the present application teaches a flash memory device comprising: a memory array with primary and redundant memory cells; and redundant fuse circuitry used to replace the primary memory cells with the redundant memory cells, wherein the redundant fuse circuitry stores an error code indicating a type of defect in addition to a defect location. Whereas Patent '932 teaches a flash memory device comprising: a memory array; a state machine to control operations to the memory array; and a defect register to store data indicating a type of defect, wherein the state machine increments row addresses during an erase operation based on the type of defect stored in the defect register. The Examiner would like to point out that the process of correction of memory errors by replacement of redundant memory cells is well known in the art. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to correct defective memory cells by redundant cells within the method and apparatus of patent '932. This modification would have been obvious to one of ordinary skill because one of ordinary skill in the art would have recognized the process of correcting errors in memory cells by redundancy is efficient and well-Known."

Applicant disagrees and respectfully maintains that claims 1-37 of the '932 Patent do not teach or suggest a flash memory device comprising: a memory array with primary and redundant memory cells; and redundant fuse circuitry used to replace the primary memory cells with the redundant memory cells, wherein the redundant fuse circuitry stores an error code indicating a type of defect in addition to a defect location and contends that the flash memory device of claims 1-30 of the Present Application differs from that disclosed in claims 1-37 of the '932 Patent. In particular, Applicant respectfully maintains that claims 1-37 of the '932 Patent do not teach or suggest replacing multiple types of defective elements from the memory array, only replacing a defective row with a redundant row, and that the Examiner is impermissibly relying

on the disclosure to provide the other missing defective elements, such as defective columns. MPEP § 804 states, "When considering whether the invention defined in a claim of an application is an obvious variation of the invention defined in the claim of a patent, the disclosure of the patent may not be used as prior art." The Applicant therefore maintains that claims 1-37 f the '932 Patent do not teach or suggest all elements of claims 1-30.

Therefore, Applicant maintains that claims 1-30 of the present application are patentably distinct from claims 1-37 of the '932 Patent because claims 1-30 of the present application require non-obvious limitations not included in claims 1-37 of the '932 Patent. The Applicant therefore respectfully requests that the rejection of claims 1-30 under the judicially created doctrine of obviousness-type double patenting be withdrawn and claims 1-30 allowed.

Claim Rejections Under 35 U.S.C. § 103

Claims 1-30 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Nozoe et al. (U.S. Patent No. 6,351,412) in view of Mizuno et al. (U.S. Patent No. 5,357,473). Applicant respectfully traverses this rejection and feels that claims 1-30 are allowable for the following reasons.

Applicant respectfully disagrees and continues to maintain that Nozoe et al. only discloses a non-volatile memory device that, to increase the speed of read access, outputs the uncorrected data read from the memory array while error correction code (ECC) stored with the data is processed to check for data errors (generate syndromes). If an error is detected, the memory device of Nozoe et al. indicates the error and allows the system to re-read the corrected data if it is so desired.

The Applicant also continues to respectfully maintain that the spare memory sections and a defective address register that allowed defective bits of the memory array to be replaced and cited by the Examiner (Nozoe et al. Column 10, Lines 32-37), does not disclose or suggest storing data on the type of defect in the address location it is replacing as claimed in the Present Application; it only teaches replacing the location with a spare/redundant memory location and storing the address of replaced location to allow future accesses to be redirected to the replacement. The Applicant also notes that an ECC code and ECC checking circuitry are used to error check the data the ECC code is stored with in the memory array and allows for selective error detection and correction and would be recognized as such by one skilled in the art. The

Applicant therefore asserts that the ECC codes and ECC circuitry are not related to the defective address location register or address redirection circuitry and does not redirect the memory read access to a different location and does not store error data or type of error, as seems to be asserted by the Examiner. *See, e.g.*, Nozoe et al., column 1, line 62 to column 2, line 2, column 2, lines 33-67, and column 10, lines 32-37.

Applicant therefore respectfully submits that Nozoe et al. does not teach or suggest a non-volatile memory device with a memory array having primary and redundant memory cells, where redundant fuse circuitry of the memory device is used to replace the primary memory cells with the redundant memory cells and the redundant fuse circuitry stores an error code indicating a type of defect in the primary memory cells in addition to the address of the defective primary memory cells in the array. Applicant thus respectfully submits that Nozoe et al. does not teach or suggest all elements of the Applicant's claimed invention.

Applicant also respectfully maintains that Mizuno et al. discloses a semiconductor system and memory device that replaces both whole defective addresses and single defective bits in its memory array. In doing so it stores defective addresses and the individual defective bit addresses of defects in either a defective address register or a defective bit register and as such, does not disclose or suggest storing data or a code indicating the type of defect in the address location it is replacing as claimed in the Present Application. Applicant also maintains that Mizuno et al. discloses testing the memory array and discovered defects to replace with a redundant address or replacement bit, but does not store the type of error, just that an address must be replaced. *See, e.g.,* Mizuno et al., Figure 3, column 3, lines 19-59; column 4, lines 26-53; column 8, line 33 to column 9, line 39 and column 9, line 64 to column 10, line 47. As such, Applicant maintains that Mizuno et al. does not disclose or suggest storing a defect error code with the address or bit address being replaced and therefore does not teach or disclose all elements of Applicant's claimed invention.

In addition to the above arguments, the Applicant further contends that there is no motivation or suggestion to modify the reference, Mizuno et al., in this manner. Specifically, Applicant contends that to modify Mizuno et al. to provide storage of defect types would require a modification of Mizuno et al.'s defective address register and/or defective bit address register to allow storage of defect type as well as the defect address location. Mizuno et al. expressly teaches away from this and only states that "[t]he system further including a defect address memory for storing information regarding an address where at least one defective bit exists among addresses consisting of one or more bits and regarding a substitute address to be

substituted for the address; and a defect address manipulating circuit for substituting the substitute address for the address where the defective bit exists in accordance with an output of the defect address memory. The semiconductor storage system may further include: a defective bit memory for storing positional information of the defective bit existing at the address to be output; an alternative semiconductor storage element for providing alternative storage of the defective bit; and a defective data manipulating circuit for replacing an output from the defective bit with an output from the defect alternative semiconductor storage element in accordance with an output of the defective bit memory." *See, e.g.*, Mizuno et al., column 3, lines 19-44; column 7, lines 41-48. Applicant also finds no motivation or suggestion to modify the operation of Mizuno et al. expressly or impliedly contained in the Mizuno et al. reference, and the Office Action does not provide a convincing line of reasoning as to why an artisan would have found the claimed invention to have been obvious in light of the teachings of the reference. Applicant thus submits that the Office has failed to meet its burden of establishing a *prima facie* case of obviousness. *See* MPEP § 706.02(j) ("The initial burden is on the examiner to provide some suggestion of the desirability of doing what the inventor has done. 'To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references.'").

If, alternatively, the Examiner is arguing that such storage of an error code in Mizuno et al. is inherent or is taking Official Notice of such, Applicant herein traverses any such assertion and requests a reasoned argument or secondary reference to support any such position by the Examiner.

Applicant therefore respectfully submits that Mizuno et al. does not teach or suggest storing an error code indicating the type of defect of the defective primary memory cells in the array, in addition to storing the address. Applicant thus respectfully submits that combining Nozoe et al. with Mizuno et al. does not teach or suggest the Applicant's claimed invention, as maintained by the Examiner. Applicant therefore respectfully contends that Mizuno et al. and Nozoe et al. do not teach or suggest all elements of the Applicant's claimed, either alone or in combination.

Applicant's claim 1 recites, in part, "redundant fuse circuitry used to replace the primary memory cells with the redundant memory cells, wherein the redundant fuse circuitry stores an error code indicating a type of defect in addition to a defect location." As detailed above,

Applicant submits that both Nozoe et al. and Mizuno et al. fail to teach or suggest such a flash memory device having redundant fuse circuitry used to replace the primary memory cells with the redundant memory cells, wherein the redundant fuse circuitry stores an error code indicating a type of defect, either alone or in combination. As such, Nozoe et al. and Mizuno et al. fail to teach or suggest all elements of independent claim 1, either alone or in combination.

Applicant's claim 8 recites, in part, "at least one register to store an address of a defective element in a primary memory array, the register having at least one data bit to store an error code in addition to a defect location." As detailed above, Applicant submits that both Nozoe et al. and Mizuno et al. fail to teach or suggest such a flash memory device having at least one register to store an address of a defective element in a primary memory array, the register having at least one data bit to store an error code, either alone or in combination. As such, Nozoe et al. and Mizuno et al. fail to teach or suggest all elements of independent claim 8, either alone or in combination.

Applicant's claim 12 recites, in part, "a register for each redundant array element to store an address of a defective element in the memory array, each register further stores an error code." As detailed above, Applicant submits that both Nozoe et al. and Mizuno et al. fail to teach or suggest such a flash memory device having a register for each redundant array element to store an address of a defective element in the memory array, each register further stores an error code, either alone or in combination. As such, Nozoe et al. and Mizuno et al. fail to teach or suggest all elements of independent claim 12, either alone or in combination.

Applicant's claim 17 recites, in part, "a register for each redundant row to store the address of the associated defective row, each register further stores an error code, wherein the error code indicates the type of error the redundant row is used to correct." As detailed above, Applicant submits that both Nozoe et al. and Mizuno et al. fail to teach or suggest such a flash memory device having a register for each redundant row to store the address of the associated defective row, each register further stores an error code, wherein the error code indicates the type of error the redundant row is used to correct, either alone or in combination. As such, Nozoe et al. and Mizuno et al. fail to teach or suggest all elements of independent claim 17, either alone or in combination.

Applicant's claim 20 recites, in part, "a register for each redundant column to store the address of the associated defective column, each register having at least one extra bit to store an error code, wherein the error code indicates the type of error in the at least one defective column." As detailed above, Applicant submits that both Nozoe et al. and Mizuno et al. fail to

teach or suggest such a flash memory device having a register for each redundant column to store the address of the associated defective column, each register having at least one extra bit to store an error code, wherein the error code indicates the type of error in the at least one defective column, either alone or in combination. As such, Nozoe et al. and Mizuno et al. fail to teach or suggest all elements of independent claim 20, either alone or in combination.

Applicant's claim 24 recites, in part, "a register for each redundant row to store the address of an associated defective row, each register further having at least one bit to store an error code, wherein the error code indicates the type of defect in the associated defective row." As detailed above, Applicant submits that both Nozoe et al. and Mizuno et al. fail to teach or suggest such a flash memory device having a register for each redundant row to store the address of an associated defective row, each register further having at least one bit to store an error code, wherein the error code indicates the type of defect in the associated defective row, either alone or in combination. As such, Nozoe et al. and Mizuno et al. fail to teach or suggest all elements of independent claim 24, either alone or in combination.

Applicant's claim 28 recites, in part, "a register for each redundant row and each redundant column to store the addresses of associated defective rows and columns, each register having at least one bit to store an error code, wherein the error code indicates the type of defect the redundant row or column is used to correct." As detailed above, Applicant submits that both Nozoe et al. and Mizuno et al. fail to teach or suggest such a flash memory device having a register for each redundant row and each redundant column to store the addresses of associated defective rows and columns, each register having at least one bit to store an error code, wherein the error code indicates the type of defect the redundant row or column is used to correct, either alone or in combination. As such, Nozoe et al. and Mizuno et al. fail to teach or suggest all elements of independent claim 28, either alone or in combination.

Applicant respectfully contends that the Examiner has not met the burden of establishing a *prima facie* case of obviousness in regards to claims 1, 8, 12, 17, 20, 24 and 28, and, in addition, that claims 1, 8, 12, 17, 20, 24 and 28 as pending have been shown to be patentably distinct from the cited references Nozoe et al. and Mizuno et al. either alone or in combination, or alone or in combination with the Examiner's taking of official notice or inherency. As claims 2-7, 9-11, 13-16, 18-19, 21-23, 25-27 and 29-30 depend from and further define claims 1, 8, 12, 17, 20, 24 and 28, respectively, they are also believed to be allowable. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 1-30.

CONCLUSION

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2207.

Respectfully submitted,

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